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EXAMINER	
KRAIG, WILLIAM F	

ART UNIT	PAPER NUMBER
2892	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/790,211	AOKI, TAKAAKI	
	Examiner	Art Unit	
	WILLIAM F. KRAIG	2892	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 December 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-16 and 26-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-16 and 26-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. The numbering of claims is not in accordance with 37 CFR 1.126 which requires the original numbering of the claims to be preserved throughout the prosecution. When claims are canceled, the remaining claims must not be renumbered. When new claims are presented, they must be numbered consecutively beginning with the number next following the highest numbered claims previously presented (whether entered or not).

Misnumbered claims 34-43 have been renumbered 33-42.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 5, 7, 11-13, 32 and 37-42 (as renumbered by Examiner) are rejected under 35 U.S.C. 103(a) as being unpatentable over Hshieh (U.S. Patent # 6262453) in view of Aoki et al. (U.S. Patent # 6469345).

Regarding claims 1 and 7, Figs. 3A-3M of Hshieh disclose a method for manufacturing a semiconductor device comprising the steps of:

forming a trench (115) having an inner wall (inner wall of trench 115) in a substrate (110);

forming an insulation film (120) on the inner wall of the trench (Fig. 3C);

forming a conductive film (125) in the trench on the insulation film (Fig. 3I);

forming an interlayer (145) over the conductive film (125); and

annealing the substrate at an annealing temperature (Col. 6, Lines 20-25) after the step of forming the conductive film 125, wherein the annealing temperature is higher than 1150 degrees Celsius and is equal to or less than 1200 degrees Celsius (Col. 6, Lines 20-25), and wherein the annealing of the substrate is performed prior to forming the interlayer 145 (see Figs. 3A-3M);

wherein the trench includes a sidewall with upper and lower portions (see Figs. 3A-3M).

The claim to the annealing process being for improvement of reliability of the insulation film and so that a damage in the insulation film is removed at the annealing temperature are purely functional limitations. It is well known that similar processes have similar characteristic results and functions. Thus, as the device of Hshieh meets the methodological limitations of this claim, it should also exhibit similar functional characteristics.

Hshieh, however, fails to teach the substrate being made specifically from silicon, the insulation film including an oxide-nitride-oxide film and upper and lower oxide films, wherein the oxide-nitride-oxide film is disposed on the sidewall of the trench, the upper oxide film is disposed on the upper portion of the trench, and the lower oxide film is disposed on the lower portion of the trench, wherein the oxide-nitride-oxide film includes a silicon oxide film, a silicon nitride film and another silicon oxide film, and wherein the upper and lower oxide films are made of silicon oxide.

Aoki et al. teaches a similar semiconductor device wherein the substrate (Aoki et al., Fig. 2H (1, 2, 3)) is made of silicon (Aoki et al., Col. 2, Lines 48-50), and further:

wherein the insulation film (Aoki et al., Fig. 2C (7a)) includes an oxide-nitride-oxide film (Aoki et al., Fig. 2H (7a, 7b, 7c)) and upper (Aoki et al., Fig. 2H (7d)) and lower oxide films (Aoki et al., Fig. 2H (7e)),

wherein the oxide-nitride-oxide film (Aoki et al., Fig. 2H (7a, 7b, 7c)) is disposed on the sidewall of the trench (Aoki et al., Fig. 2H (side walls of trench (6), having oxide film (7a) disposed thereon)), the upper oxide film (Aoki et al., Fig. 2H (7d)) is disposed on the upper portion of the trench (Aoki et al., Fig. 2H (upper portion of trench (6), having oxide film (7d) disposed thereon)), and the lower oxide film (Aoki et al., Fig. 2H (7e)) is disposed on the lower portion of the trench (Aoki et al., Fig. 2H (lower portion of trench (6), having oxide film (7e) disposed thereon)),

wherein the oxide-nitride-oxide film (Aoki et al., Fig. 2H (7a, 7b, 7c)) includes a silicon oxide film (Aoki et al., Fig. 2H (7a)), a silicon nitride film (Aoki et al., Fig. 2H (7b)) and another silicon oxide film (Aoki et al., Fig. 2H (7c)) (Aoki et al., Col. 2, Lines 57-62), and

wherein the upper (Aoki et al., Fig. 2H (7d)) and lower (Aoki et al., Fig. 2H (7e)) oxide films are made of silicon oxide (Aoki et al., Col. 2, Lines 66-67).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the ONO film of Aoki et al. into the device of Hshieh. The ordinary artisan would have been motivated to modify Hshieh in the above manner for

the purpose of providing a structure having a high withstand voltage (Aoki et al., Col. 3, Lines 20-30).

Regarding claim 5, Hshieh and Aoki et al. disclose the method according to claim 1, wherein the conductive film (Hshieh, Figs. 3A-3M (125)) is made of doped poly crystalline silicon (Hshieh, Col. 6, Lines 10-20), and wherein the insulation film (Hshieh, Figs. 3A-3M (125)) (Aoki et al., Fig. 2C (7)) is made of silicon oxide and silicon nitride (Aoki et al., Col. 2, Lines 57-62).

Regarding claim 11, Hshieh and Aoki et al. disclose the method according to claim 1, wherein the conductive film is a gate electrode, further comprising:

implanting an impurity into the substrate with using the gate electrode as a mask after the step of forming the gate electrode (see Fig. 3J) (Hshieh, Col. 6, Lines 24-28);

performing a thermal diffusion process (Hshieh, Col. 6, Lines 28-33) for diffusing the impurity so that a source region (Hshieh, Figs. 3A-3M (140)) adjacent to the trench and disposed on a surface of the substrate is formed (see Fig. 3K);

wherein the annealing is performed prior to performing the thermal diffusion process (Hshieh, Col. 6, Lines 20-35).

Regarding claim 12, Hshieh and Aoki et al. disclose the method according to claim 11, wherein the thermal diffusion process is performed at a process temperature (1000-1200 degrees Celsius); and

wherein the annealing temperature (1000-1200 degrees Celsius) in the step of annealing is higher than the process temperature (900-1000 degrees Celsius) in the step of performing the thermal diffusion process (See Hshieh, Col. 6, Lines 20-35).

Regarding claim 13, Hshieh and Aoki et al. disclose the method according to claim 11,

wherein the insulation film (Aoki et al., Fig. 2C (7a)) includes an oxide-nitride-oxide film (Aoki et al., Fig. 2H (7a, 7b, 7c)) and upper (Aoki et al., Fig. 2H (7d)) and lower oxide films (Aoki et al., Fig. 2H (7e)),

wherein the trench (Aoki et al., Fig. 2B (6)) includes a sidewall (Aoki et al., Fig. 2H (side walls of trench (6), having oxide film (7a) disposed thereon)) and upper (Aoki et al., Fig. 2H (upper portion of trench (6), having oxide film (7d) disposed thereon)) and lower portions (Aoki et al., Fig. 2H (lower portion of trench (6), having oxide film (7e) disposed thereon)),

wherein the oxide-nitride-oxide film (Aoki et al., Fig. 2H (7a, 7b, 7c)) is disposed on the sidewall of the trench (Aoki et al., Fig. 2H (side walls of trench (6), having oxide film (7a) disposed thereon)), the upper oxide film (Aoki et al., Fig. 2H (7d)) is disposed on the upper portion of the trench (Aoki et al., Fig. 2H

(upper portion of trench (6), having oxide film (7d) disposed thereon)), and the lower oxide film (Aoki et al., Fig. 2H (7e)) is disposed on the lower portion of the trench (Aoki et al., Fig. 2H (lower portion of trench (6), having oxide film (7e) disposed thereon)),

wherein the oxide-nitride-oxide film (Aoki et al., Fig. 2H (7a, 7b, 7c)) includes a silicon oxide film (Aoki et al., Fig. 2H (7a)), a silicon nitride film (Aoki et al., Fig. 2H (7b)) and another silicon oxide film (Aoki et al., Fig. 2H (7c)) (Aoki et al., Col. 2, Lines 57-62), and

wherein the upper (Aoki et al., Fig. 2H (7d)) and lower (Aoki et al., Fig. 2H (7e)) oxide films are made of silicon oxide (Aoki et al., Col. 2, Lines 66-67).

Regarding claim 32, Hshieh and Aoki et al. disclose the method according to claim 1, wherein the interlayer (Hshieh, Figs. 3A-3M (145)) comprises BPSG (Hshieh, Col. 6, Lines 50-52).

Regarding claim 37, Hshieh and Aoki et al. disclose the method according to claim 11, wherein the source region (Hshieh, Figs. 3A-3M (140)) is an N+ source region (see Figs. 3A-3M of Hshieh).

Regarding claim 38, Hshieh and Aoki et al. disclose the method according to claim 11, wherein the performing of the thermal diffusion process for diffusing the

impurity also operates so that a body region (Hshieh, Figs. 3A-3M (130)) is formed adjacent to the source region in the substrate (see Figs. 3A-3M of Hshieh).

Regarding claim 39, Hshieh and Aoki et al. disclose the method according to claim 39, wherein the annealing is performed prior to performing the thermal diffusion process (Hshieh, Col. 6, Lines 20-35).

Regarding claim 40, Hshieh and Aoki et al. disclose the method according to claim 40, wherein the source region (Hshieh, Figs. 3A-3M (140)) is an N+ source region, and wherein the body region (Hshieh, Figs. 3A-3M (130)) is a P type body region (see Figs. 3A-3M of Hshieh).

Regarding claim 41, Hshieh and Aoki et al. disclose the method according to claim 11, further comprising forming an interlayer (Hshieh, Figs. 3A-3M (145)) over the gate electrode (Hshieh, Figs. 3A-3M (125)), wherein the annealing of the substrate is performed prior to forming the interlayer (Hshieh, Col. 6, Lines 20-53)

Regarding claim 42, Hshieh and Aoki et al. disclose the method according to claim 42, wherein the interlayer (Hshieh, Figs. 3A-3M (145)) comprises BPSG (Hshieh, Col. 6, Lines 50-52)..

3. Claims 2, 4, 6, 8-10, 14, 15 and 33-36 (as renumbered by Examiner) are rejected under 35 U.S.C. 103(a) as being unpatentable over Hshieh (U.S. Patent # 6262453) in view of Aoki et al. (U.S. Patent # 6469345) as applied to claims 1, 5, 7, 11-13, 32 and 37-42, above, and further in view of Inagawa et al. (U.S. Patent # 6455378).

Regarding claims 2, 4, 6, 8 and 14, Hshieh and Aoki et al. disclose the method according to claims 1, 5, 7 and 13 (see rejection above), further comprising the steps of:

forming a source region (Hshieh, Figs. 3A-3M (140)) having a contact surface between the source region and the substrate (Hshieh, Figs. 3A-3M, (contact surface is bottom surface of source region (140))), which is disposed near the trench (Hshieh, Figs. 3A-3M (115)) and is almost parallel to the substrate (see Figs. 3A-3M of Hshieh),

wherein the insulation film (Aoki et al., Fig. 2C (7)) (Hshieh, Figs. 3A-3M (120)) includes an oxide-nitride-oxide film (Aoki et al., Fig. 2H (7a, 7b, 7c)) and upper (Aoki et al., Fig. 2H (7d)) and lower oxide films (Aoki et al., Fig. 2H (7e)),

wherein the conductive film (Aoki et al., Fig. 2H (8)) in the trench provides a gate electrode (Aoki et al., Col. 4, Lines 26-28),

Hshieh and Aoki et al., however, fail to disclose the gate electrode including a canopy for covering the upper oxide film so that the gate electrode has a T-shaped cross section, and the canopy of the gate electrode having an edge, which is disposed at a predetermined distance from an edge of an opening of the trench, and the predetermined distance being predetermined not to prevent the source region from forming.

Fig. 16(c) of Inagawa et al. teaches a gate electrode (3(3b)) including a canopy for covering the upper oxide film so that the gate electrode has a T-shaped cross section (See Fig. 16(c)), the canopy of the gate electrode having an edge (edge of gate electrode (3(3b)) coincident with layer (2b)), said edge being disposed at a predetermined distance (distance between edge of gate electrode (3(3b)) coincident with layer (2b) and edge of trench opening (see Fig. 16(c))) from an edge of an opening of the trench, wherein the predetermined distance (distance between edge of gate electrode (3(3b)) coincident with layer (2b) and edge of trench opening (see Fig. 16(c))) is predetermined not to prevent the source region (6) from forming (Col. 11, Lines 59-60).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the gate electrode of Inagawa et al. into the method of Hshieh and Aoki et al. The ordinary artisan would have been motivated to modify Hshieh and Aoki et al. in the above manner for the purpose of having more control over the depth of the source region (Inagawa et al., Col. 11, Lines 54-60).

Regarding claim 9, Hshieh, Aoki et al. and Inagawa et al. disclose the method according to claim 1, wherein the device includes a cell region (Inagawa et al, Fig. 2 (area containing transistor cells (Q))) and a gate lead wire region (Inagawa et al., Fig. 2 (area containing gate line (3GL)), wherein the cell region (Inagawa et al, Fig. 2 (area containing transistor cells (Q))) includes a plurality of cells (Inagawa et al, Fig. 2 (Q)), each of which works as a transistor (Inagawa et al., Col. 6, Lines 6-14), and wherein the

gate lead wire region (Inagawa et al., Fig. 2 (area containing gate line (3GL)) includes a gate lead wire (Inagawa et al, Fig. 2 (3GL)) (Inagawa et al., Col. 6, Lines 59-60).

Regarding claim 10, Hshieh, Aoki et al. and Inagawa et al. disclose the method according to claim 9, wherein the transistor (Inagawa et al, Fig. 2 (Q)) (Inagawa et al., Col. 6, Lines 6-14) is an N channel type MOSFET, a P channel type MOSFET or an IGBT (Aoki et al., Col. 2, Lines 44-47).

Regarding claim 33, Hshieh, Aoki et al. and Inagawa et al. disclose the method according to claim 2, wherein the annealing is performed prior to forming the source region (Hshieh, Figs. 3A-3M (140))(Hshieh, Col. 6, Lines 20-35).

Regarding claim 34, Hshieh, Aoki et al. and Inagawa et al. disclose the method according to claim 2, wherein the source region (Hshieh, Figs. 3A-3M (140)) is an N+ source region (see Figs. 3A-3M of Hshieh).

Regarding claim 35, Hshieh, Aoki et al. and Inagawa et al. disclose the method according to claim 2, further comprising forming a body (Hshieh, Figs. 3A-3M (130)) region in the substrate and adjacent to the source region (see Figs. 3A-3M of Hshieh).

Regarding claim 36, Hshieh, Aoki et al. and Inagawa et al. disclose the method according to claim 35, wherein the source region (Hshieh, Figs. 3A-3M (140)) is an N+

source region, and wherein the body region (Hshieh, Figs. 3A-3M (130)) is a P type body region (see Figs. 3A-3M of Hshieh)

4. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hshieh in view of Aoki et al. in view of Inagawa et al., as applied to claims 2, 4, 6, 8-10, 14 and 33-36 above, and further in view of Pan et al. (U.S. Patent # 6159781).

Regarding claim 15, Hshieh, Aoki et al. and Inagawa et al. disclose the method according to claim 14, but fail to disclose the distance between the edge of the canopy and the edge of the opening of the trench being, specifically, in a range between 0.05 micrometers and 0.1 micrometers.

It would have been obvious to one of ordinary skill in the art to cause the distance between the edge of the canopy and the edge of the opening of the trench to be in a range between .05 micrometers and .1 micrometers. The claim to the specified range in the distance between the edge of the canopy and the edge of the opening on the trench constitutes an optimization of ranges. *In re Huang*, 100 F.3d 135, 40 USPQ2d 1685, 1688 (Fed. Cir. 1996). The ordinary artisan would have been motivated to modify Hshieh, Aoki et al. and Inagawa et al. in the above manner for the purpose of decreasing gate capacitance (Pan et al., Col. 1, Lines 35-40).

5. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hshieh (U.S. Patent # 6262453) in view of Aoki et al. (U.S. Patent # 6469345) as applied to

claims 1, 5, 7, 11-13, 32 and 37-42, above, and further in view of Narwankar et al. (U.S. Patent # 6218300).

Regarding claim 16, Hshieh and Aoki et al. disclose the method according to claim 11, but fail to disclose the substrate being annealed in an inert gas atmosphere in the step of annealing.

Narwankar et al. teaches a method of annealing wherein an inert gas is included in the anneal gas stream (Narwankar et al., Col. 6, Lines 30-35)

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the inert gas method of Narwankar et al. into the method of Hshieh and Aoki et al. The ordinary artisan would have been motivated to modify Hshieh and Aoki et al. in the above manner for the purpose of preventing recombination of the active atomic species (Narwankar et al., Col. 6, Lines 30-35).

6. Claims 26-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hshieh (U.S. Patent # 6262453) in view of Aoki et al. (U.S. Patent # 6469345) as applied to claims 1, 5, 7, 11-13, 32 and 37-42, above, and further in view of Williams (U.S. Patent # 5814858) with evidence provided by Gioia (U.S. Patent # 4874713).

Regarding claims 26 and 29, Hshieh and Aoki et al. disclose the method according to claims 1 and 11, but fail to disclose forming an oxide film on the conductive film before the annealing of the substrate.

Figs. 11A-11J of Williams teach a similar method of forming a semiconductor device wherein an oxide film (Williams, Fig. 11D (1102)) is formed on a similar

conductive film (Williams, Fig. 11D (702)) before a similar annealing of the substrate (Williams, Col. 7, Lines 35-47).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the oxide film of Williams into the device of Hshieh and Aoki et al. The ordinary artisan would have been motivated to modify Hshieh and Aoki et al. in the above manner for the purpose of protecting the surface of the substrate from implant damage (Gioia, Col. 3, Lines 40-45).

Regarding claims 27 and 30, Hshieh, Aoki et al. and Williams (with evidence provided by Gioia) disclose the method according to claims 26 and 29, wherein the oxide film (Williams, Fig. 11D (1102)) covers the conductive film (Williams, Fig. 11D (702)) and the substrate ((Williams, Fig. 11D (704)).

Regarding claims 28 and 31, Hshieh, Aoki et al. and Williams (with evidence provided by Gioia) disclose the method according to claims 27 and 30, wherein the annealing of the substrate is performed for between 10 minutes and 30 minutes (Hshieh, Col. 6, Lines 20-25).

Response to Arguments

7. Applicant's arguments with respect to all claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The cited art discloses similar semiconductor devices.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to WILLIAM F. KRAIG whose telephone number is (571)272-8660. The examiner can normally be reached on Mon-Fri 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thao X. Le can be reached on 571-272-1708. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Lex Malsawma/
Primary Examiner, Art Unit 2892

/W. F. K./
Examiner, Art Unit 2892
02/11/2008